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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Philip Neaves	Attorney Docket No.: 501340.02
Filed	: Concurrently herewith	
Title	: STRUCTURE AND METHOD FOR FORMING A CAPACITIVELY COUPLED CHIP-TO-CHIP SIGNALING INTERFACE	

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Sir:

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In accordance with C.F.R. § 1.55(a)(2), enclosed herewith is a certified copy of the United Kingdom Patent Application No. 0323992.8 filed October 13, 2003.

Respectfully submitted,

Date: 2/12/04

By: _____

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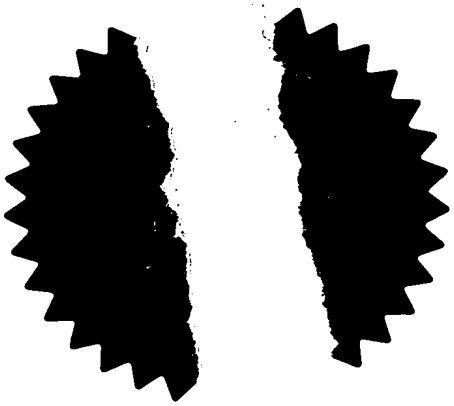

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2. Patent application number
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Micron Technology, Inc.
8000 South Federal Way
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Idaho
83706-9632
United States of America

Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation — 05933965003

4. Title of the invention — Structure and Method for Forming a Capacitively Coupled Chip-to-Chip Signalling Interface

5. Name of your agent *(if you have one)*

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STRUCTURE AND METHOD FOR FORMING A CAPACITIVELY COUPLED CHIP-TO-CHIP SIGNALING INTERFACE

TECHNICAL FIELD

The present invention is directed to a system-in-package device, and more particularly, to a system and method for providing capacitively-coupled signaling in a system-in-package device.

BACKGROUND OF THE INVENTION

Traditional semiconductor integrated circuit technology is commonly used to integrate various electronic circuits onto a common semiconductor substrate to form an electronic system, or subsystem. The traditional approach to integrating circuits into a system often has process, manufacturing and design limitations which present difficulties when certain electronic circuits are integrated onto a common semiconductor substrate. A recently developed integration technology commonly referred to as system-in-package (SiP) technology attempts to overcome at least some of the limitations of traditional semiconductor integration methods by interconnecting multiple discrete and individually fabricated semiconductor systems on a common substrate and encapsulating the complete system in a common package. Accordingly, SiP allows a variety of device technologies to be integrated into a single package that would otherwise be difficult and expensive to fabricate using traditional integration methods. For example, SiP technology has been successfully applied in mixed signal applications, where analog and digital components are integrated onto the same chip. Such applications typically present noise immunity difficulties, since digital circuit switching commonly injects noise into the common substrate, which may corrupt sensitive analog signals. As the size of features in devices decreases and clock frequencies increase, the amount of substrate noise created by digital switching has increased dramatically.

As previously mentioned, the multiple discrete systems of a SiP are electrically coupled together to form a system and, as is well known in the art of digital electronics, many of the multiple systems communicate with one another by transmitting digital information in the form of electrical signals. Typically, even analog-based systems in the SiP generally have analog signals converted into the digital domain. The electrical signals transmitted between the multiple systems generally represent a serial data stream where the data is represented by binary states having discrete levels of amplitude or phase, as well known. Multiple electrical signals are transmitted in parallel to transmit data of a data width, with each signal representing one bit of the width of data. In transmitting the data, the electrical signal may be distorted by various phenomena, such as noise, signal strength variations, phase shift variations, and the like. Moreover, multiple individual devices generally interact in a SiP, and the various devices may operate at different voltage levels that may cause undesired electrical currents to flow from one system to another, which generally contributes to excess power consumption. Additionally, the undesired current may be sufficiently large to damage to the devices.

Consequently, SiP devices have employed capacitively coupled signaling between the multiple systems to filter noise from the electrical signals and also prevent current flow between devices operating in different voltage domains. Figure 1 illustrates a capacitively coupled signaling system having a capacitively coupled data bus 100 that is n-bits wide that may be used to transmit data signals D_OUT0-D_OUTn. The data bus 100 includes output driver circuits, or transmitters 102 of the transmitting device capacitively coupled through capacitors 106 to input buffer circuits, or receivers 104 at the receiving device. The received data has been represented by the received data signals D_IN0-DINn. As shown in Figure 1, the data bus 100 has been illustrated as a uni-directional data bus, with the transmitters 102 representing a transmitting device and the receivers 104 representing a receiving device. However, it will be appreciated that the data bus 100 has been illustrated in this manner by way of example, and that the data bus 100 can be a bi-directional data bus as well.

Lower power may be consumed when utilizing capacitively coupled signaling since there is only minimal leakage current between devices. Capacitively coupled signaling is also insensitive to voltage domains, allowing operation without the need for level shifting. Specifically, a capacitively coupled signaling system permits an AC component of a signal to be transferred, while blocking a DC component of the signal. Additionally, circuits designed for protection from electrostatic discharge (ESD) are no longer necessary where the signaling is entirely contained within the SiP device. Circuits dedicated to ESD protection, usually consisting of diode networks in various configurations, add complexity to the terminal regions of a device, and compete for "real estate" on the device substrate. Load requirements on output circuitry can also be relaxed compared with conventional off-die signaling because the need to drive signals external to the device package are eliminated for those signals that remain internal to the SiP device.

In forming capacitively coupled signaling systems, discrete passive components have been used to connect the signal terminals of the different systems, such as discrete capacitors, resistors, and the like. However, when discrete components are used, some of the foregoing advantages associated with a capacitively coupled signaling system are reduced. For example, when a signal pad is wire bonded to a discrete passive component that further extends to another signal pad, parasitic effects are generally introduced. Additionally, when several discrete components are included in a SiP, an increased form factor is generally developed, since the additional components must be accommodated. Passive components can be integrated into each discrete system, thereby avoiding issues with having additional passive components included in the SiP, but even when the passive components are integrated into the SiP, the need to have wires coupling the signal pads of the discrete systems cannot be avoided. As noted above, bonding wires can cause undesirable parasitic loading effects. Therefore, there is a need in the art for an alternative capacitively coupled signaling structure and a method for forming a capacitively coupled structure.

SUMMARY OF THE INVENTION

The present invention is directed to a system and method for providing capacitively-coupled signaling in a system-in-package (SiP) device. In one aspect, the SiP device includes a first semiconductor device and an opposing second semiconductor device spaced apart from the first semiconductor device, a dielectric layer interposed between the first semiconductor device and the second semiconductor device, a first conductive pad positioned in the first semiconductor device, and a second conductive pad positioned in the second semiconductor device that is configured to capacitively communicate signals from the second semiconductor device to the first semiconductor device. In another aspect, a method of forming a SiP device includes forming a first conductive signal pad on a surface of a first semiconductor device, forming a second conductive signal pad on a surface of a second semiconductor device, and interposing a dielectric layer between the first semiconductor device and the second semiconductor device that separates the first conductive signal pad and the second conductive signal pad.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic view of a capacitively coupled signaling system according to the prior art.

Figure 2 is a partial isometric and cross-sectional view of a capacitively coupled SiP according to an embodiment of the invention.

Figure 3 is a partial isometric and cross-sectional view of a capacitively coupled SiP according to another embodiment of the invention.

Figure 4 is a partial isometric and cross-sectional view of a capacitively coupled SiP according to still another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is generally directed to a system-in-package device, and more particularly, to a system and method for providing capacitively-coupled signaling in a system-in-package device. Many of the specific details of certain

embodiments of the invention are set forth in the following description and in Figures 2-4 to provide a thorough understanding of such embodiments. One skilled in the art will understand, however, that the present invention may be practiced without several of the details described in the following description. Moreover, in the description that follows, it is understood that the figures related to the various embodiments are not to be interpreted as conveying any specific or relative physical dimension. Instead, it is understood that specific or relative dimensions related to the embodiments, if stated, are not to be considered limiting unless the claims specifically state otherwise.

Figure 2 is a partial isometric and cross-sectional view of a capacitively coupled SiP 200 according to an embodiment of the invention. The SiP 200 includes a first semiconductor device 210 and a second semiconductor device 220 that is spaced apart from the first semiconductor device 210 by a dielectric layer 230. The first semiconductor device 210 includes a signal pad 212 that is coupled to the transmitter 102 that transmits a data signal D_OUT0 to the signal pad 212. The first semiconductor device 210 further includes a signal pad 214 that is coupled to the transmitter 102 that transmits a data signal D_OUT1 to the signal pad 214. In a similar manner, the second semiconductor device 220 includes a signal pad 222 that is coupled to the receiver 104 that transmits a data signal D_IN0 from the signal pad 222. The second semiconductor device 220 further includes a signal pad 224 that is coupled to the receiver 104 that transmits a data signal D_IN1 from the signal pad 224. The pads 212 and 222, and the pads 214 and 224 are positioned within the semiconductor devices 210 and 220 to permit the data signals to be exchanged between the devices 210 and 220 through the dielectric layer 230 by capacitive coupling. Although Figure 2 illustrates only four signal pads that are configured to capacitively transfer signals between the first semiconductor device 210 and the second semiconductor device 220, it is understood that the capacitively coupled SiP 200 may include more than four similarly configured pads, or as few as two signal pads.

The signal pad 212 of the first semiconductor device 210 and the pad 222 of the second semiconductor device 220 are approximately mutually in alignment, as shown in Figure 2, so that the capacitive coupling between the semiconductor

devices 210 and 220 may be maximized. Similarly, the pads 214 and 224 are approximately mutually in alignment to maximize capacitive coupling between the semiconductor devices 210 and 220. One skilled in the art will readily appreciate that the pads 212 and 222 may be configured such that the pads 212 and 222 are only in relative proximity and still achieve capacitive coupling between the devices 210 and 220. In a similar manner, the pads 214 and 224 may also be configured so that the pads 214 and 224 are only relatively proximate to one another.

Still referring to Figure 2, the dielectric layer 230 of the SiP 200 may be comprised of silicon dioxide, silicon nitride, or other alternative dielectric materials that are deposited on each of the first semiconductor device 210 and second semiconductor device 220. Alternately, and in a particular embodiment, the dielectric layer 230 may be comprised of a passivated layer formed on exposed surfaces of the first semiconductor device 210 and/or the second semiconductor device 220 during fabrication of the semiconductor devices 210 and 220. In either case, the dielectric layers formed on the first semiconductor device 210 and the second semiconductor device 220 may be combined by adhesive bonding, or by other similar methods, to form the SiP 200 shown in Figure 2. Alternately, and in another particular embodiment, the first semiconductor device 210 and the second semiconductor device 220 may be combined to form the SiP 200 by a low temperature covalent bonding process as disclosed in U.S. Patent No. 6,563,133 B1 to Tong, entitled "Method of Epitaxial-Like Wafer Bonding at Low Temperature and Bonded Structure", which is incorporated by reference herein.

The pads 212 and 214 of the first semiconductor device 210 and the pads 222 and 224 of the second semiconductor device 220 may be formed on the devices 210 and 220 by a variety of well-known methods. For example, the pads 212 and 214, and the pads 222 and 224 may be formed by depositing a layer of a dielectric material onto the first device 210 and the second device 220, masking the dielectric layers on the devices 210 and 220 and then selectively etching the dielectric layers to form recesses in the dielectric layers. A conductive material may then be deposited into the recesses to form the pads 212 and 214, and the pads 222 and 224. The pads 212, 214 and 222 and 224 may be appropriately sized to achieve a desired degree of capacitive coupling. For

example, and in one particular embodiment, the pads 212, 214, 222 and 224 have a width d_1 of approximately about 30 μm. Further, the transmitters 102 and the receivers 104 may be positioned remotely from the pads 212 and 214 and the pads 222 and 224, respectively, as shown in Figure 2. The transmitters 102 may also be formed in the first semiconductor device 210 at a location that is proximate to the pads 212 and 214. For example, the transmitters 102 may be formed at a location that is laterally adjacent to the pads 212 and 214. Alternately, the transmitters 102 may be positioned directly below and adjacent to the pads 212 and 214. In a similar manner, the receivers 102 may also be positioned at a location proximate to the pads 222 and 224, which includes positioning the receivers 102 in positions laterally adjacent to the pads 222 and 224, or directly below the pads 222 and 224.

Figure 3 is a partial isometric and cross-sectional view of a capacitively coupled SiP 300 according to another embodiment of the invention. The SiP 300 includes first and second semiconductor devices 210 and 220, respectively, which are separated by the dielectric layer 230, as in the previous embodiment. The SiP 300 further includes guard rings 310 laterally spaced apart from the pads 212, 214, 222 and 224. Each of the guard rings 310 is coupled to ground to inhibit capacitive coupling between adjacent signal pads. Accordingly, the guard rings 310 may be formed in the first semiconductor device 210 so that the pads 212 and 214 are circumferentially enclosed by the guard rings 310. Alternately, the guard rings 310 may only partially enclose the pads 212 and 214, or extend along lateral edges of the pads 21 and 214, as shown in Figure 3. Similarly, the guard rings 310 formed in the second semiconductor device 220 may circumferentially enclose the pads 222 and 224, or they may only partially enclose the pads 212 and 214, or extend along lateral edges of the pads 222 and 224, as described above. Although Figure 3 shows guard rings 310 adjacent to each of the pads 212, 214, 222 and 224, one skilled in the art will appreciate that the guard rings 310 may formed adjacent to only a portion of the signal pads in the first semiconductor device 210 and the second semiconductor device 220, while other signal pads in the devices 210 and 220 are formed without adjacent guard rings 310. Further, the guard

rings 310 may be formed in only one of the first semiconductor device 210 and the second semiconductor device 220.

Still referring to Figure 3, the guard rings 310 may be formed in the exposed surfaces of the first semiconductor device 210 and the second semiconductor device 220 by a variety of well-known processes. For example, the guard rings 310 may be formed in the dielectric material deposited on the first device 210 and the second device 220 by masking the dielectric layer so that the layer may be selectively etched to form recesses in the dielectric layers. A conductive material may then be deposited into the recesses to form the guard rings 310. In one particular embodiment, the guard rings 310 may extend into the first and second devices 210 and 220 to a depth d_3 of approximately about 0.8μm. In another particular embodiment, the guard rings 310 are spaced apart from the signal pads 212, 214, 222 and 224 by a distance d_4 of approximately about 2μm. In still another particular embodiment, the guard rings 310 have a width d_5 of approximately about 2μm.

Figure 4 is a partial isometric and cross-sectional view of a capacitively coupled SiP 400 according to still another embodiment of the inyention. The SiP 400 includes first and second semiconductor devices 210 and 220 separated by the dielectric layer 230, as in embodiments described above. The SiP 400 further includes a first ground plane 410 positioned within the first semiconductor device 210 and spaced apart from the pads 212 and 214. The first ground plane 410 may be coupled to the guard rings 310 formed in the first semiconductor device 210 to provide a low impedance path to ground for the guard rings 310. The SiP 400 also includes a ground plane 420 positioned within the second semiconductor device 220 that is spaced apart from the pads 222 and 224. The second ground plane 420 may also be coupled to the guard rings 310 formed in the second semiconductor device 220. The first ground plane 410 and the second ground plane 420 may be formed from either metallic or non-metallic conductive materials, and may be formed within the first device 210 and the second device 220 by various well-known methods. For example, in a particular embodiment, the first ground plane 410 and the second ground plane 420 may be formed by depositing a layer of copper or aluminum on the first and second devices 210 and 220

during fabrication of the devices 210 and 220. Alternately, in another particular embodiment, a layer of heavily doped polycrystalline silicon may be formed within the devices 210 and 220 to form the ground planes 410 and 420. In still another particular embodiment, the first ground plane 410 and the second ground plane 420 are spaced apart from the respective surfaces of the first semiconductor device 210 and the second semiconductor device 220 by a distance d_6 of approximately about 1.90μm.

The foregoing embodiments of the invention offer numerous advantages over the prior art. For example, the disclosed embodiments generally eliminate the need for electrostatic discharge (ESD) protection in the semiconductor devices comprising the SiP. Accordingly, the requirement to form additional devices, such as diodes or similar protective devices near the pads on a semiconductor device is eliminated, so that the device area, or "real estate" may be more efficiently utilized.

The foregoing embodiments also generally allow shorter signal paths to be established between the devices in the SiP. Accordingly, signal delay times are significantly reduced when compared to conventional wire bond or interposer coupling techniques. Undesirable parasitic effects are similarly reduced, since the inductance associated with a wire bonding element is largely eliminated. Load requirements are also advantageously reduced since a relatively low capacitive load is present between the devices. As a result, the power requirement is significantly reduced in comparison to conventional packages, where the devices are required to drive signals off one device, and onto another device. The low capacitive load between the devices further advantageously permits relatively high bandwidth operation between the devices.

Still other advantages are evident in the foregoing embodiments. For example, since the devices are capacitively coupled, the devices may be operated at different D.C. voltage levels without the requirement for D.C. voltage isolation or D.C. level shifting between the devices. Since the foregoing pad, ground ring and ground plane structures are fabricated near the exterior layers of the devices, the structures may be conveniently formed in the devices by altering only the final steps in the fabrication procedure. Accordingly, the foregoing structures may be economically incorporated into the devices by altering relatively few semiconductor device masks.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A system in package (SiP) device, comprising:

a first semiconductor device and an opposing second semiconductor device spaced apart from the first semiconductor device;

a dielectric layer interposed between the first semiconductor device and the second semiconductor device;

a first conductive pad positioned in the first semiconductor device; and

a second conductive pad positioned in the second semiconductor device and configured to capacitively communicate signals from the second semiconductor device to the first semiconductor device.

2. The system in package (SiP) device of claim 1, wherein the first conductive pad and the second conductive pad are positioned proximate to the dielectric layer.

3. The system in package (SiP) device of claim 2, wherein the first conductive pad and the second conductive pad substantially abut the dielectric layer.

4. The system in package (SiP) device of claim 1, wherein the first conductive pad and the second conductive pad are positioned in the respective first and second devices so that the first conductive pad and the second conductive pad are approximately mutually in alignment.

5. The system in package (SiP) device of claim 1, further comprising a transmitter coupled to the first conductive pad and a receiver coupled to second conductive pad.

6. The system in package (SiP) device of claim 5, wherein at least one of the transmitter and the receiver are positioned laterally adjacent to the respective first conductive pad and the second conductive pad.

7. The system in package (SiP) device of claim 5, wherein at least one of the transmitter and the receiver are positioned beneath the respective first conductive pad and the second conductive pad.

8. The system in package (SiP) device of claim 1, wherein the first conductive pad and the second conductive pad are comprised of a metal.

9. The system in package (SiP) device of claim 8, wherein the metal comprises copper.

10. The system in package (SiP) device of claim 8, wherein the metal comprises aluminum.

11. The system in package (SiP) device of claim 1, wherein the first conductive pad and the second conductive pad are comprised of polysilicon.

12. The system in package (SiP) device of claim 1, wherein the dielectric layer comprises silicon dioxide.

13. The system in package (SiP) device of claim 1, wherein the dielectric layer comprises silicon nitride.

14. The system in package (SiP) device of claim 1, further comprising a guard ring coupled to a ground potential and positioned adjacent to at least one of the first conductive pad and the second conductive pad.

15. The system in package (SiP) device of claim 14, wherein the guard ring substantially circumferentially encloses at least one of the first conductive pad and the second conductive pad.

16. The system in package (SiP) device of claim 14, further comprising a ground plane positioned adjacent to at least one of the first conductive pad and the second conductive pad, wherein the guard ring is coupled to the ground plane.

17. A system in package (SiP) device, comprising:

a first semiconductor device having a first conductive signal pad positioned adjacent to a first surface;

a second semiconductor device having a second conductive signal pad positioned adjacent to an opposing second surface, the first surface being spaced apart from the second surface by a dielectric layer, the first conductive signal pad and the second conductive pad being substantially adjacent to each other to capacitively communicate signals between the first semiconductor device and the second semiconductor device.

18. The system in package (SiP) device of claim 17, further comprising a transmitter coupled to the first conductive signal pad and a receiver coupled to second conductive signal pad.

19. The system in package (SiP) device of claim 18, wherein at least one of the transmitter and the receiver are positioned laterally adjacent to the respective first conductive signal pad and the second conductive signal pad.

20. The system in package (SiP) device of claim 18, wherein at least one of the transmitter and the receiver are positioned beneath the respective first conductive pad and the second conductive pad.

21. The system in package (SiP) device of claim 17, wherein the first conductive signal pad and the second conductive signal pad have a width of approximately about 30 μm.

22. The system in package (SiP) device of claim 17, wherein the first conductive signal pad and the second conductive signal pad have a thickness of approximately about 0.85 μm.

23. The system in package (SiP) device of claim 17, further comprising a guard ring coupled to a ground potential and positioned adjacent to at least one of the first conductive signal pad and the second conductive signal pad.

24. The system in package (SiP) device of claim 23, wherein the guard ring is laterally spaced apart from the first conductive signal pad and the second conductive signal pad by approximately about 2 μm.

25. The system in package (SiP) device of claim 24, wherein the guard ring has a lateral width of approximately about 2 μm.

26. The system in package (SiP) device of claim 23, wherein the guard ring is circumferentially disposed about the first conductive signal pad and the second conductive signal pad.

27. The system in package (SiP) device of claim 23, further comprising a ground plane coupled to the guard ring.

28. The system in package (SiP) device of claim 27, wherein the ground plane is spaced apart from the guard ring by approximately about 1.9 μm.

29. A method of forming a system in package (SiP) device, comprising:

forming a first conductive signal pad on a surface of a first semiconductor device;

forming a second conductive signal pad on a surface of a second semiconductor device; and

interposing a dielectric layer between the first semiconductor device and the second semiconductor device that separates the first conductive signal pad and the second conductive signal pad.

30. The method of claim 29, wherein interposing a dielectric layer further comprises passivating the surface of the first semiconductor device and the surface of the second semiconductor device.

31. The method of claim 30, wherein interposing a dielectric layer further comprises adhesively bonding the dielectric layer to the first semiconductor device and the second semiconductor device.

32. The method of claim 30, wherein interposing a dielectric layer further comprises combining the first semiconductor device and the second semiconductor device by a covalent bonding process.

33. The method of claim 29, further comprising forming a guard ring in at least one of the first semiconductor device and the second semiconductor device, the guard ring being laterally spaced apart from at least one of the first conductive signal pad and the second conductive signal pad.

34. The method of claim 33, further comprising positioning a ground plane adjacent to at least one of the first conductive signal pad and the second conductive signal pad; and coupling the ground plane to the guard ring.

35. The method of claim 29, further comprising coupling a transmitter to the first conductive signal pad and coupling a receiver to the second conductive signal pad.

36. The method of claim 35, further comprising forming the transmitter laterally adjacent to the first conductive signal pad and forming the receiver laterally adjacent to the second conductive signal pad.

37. The method of claim 35, further comprising forming the transmitter below the first conductive signal pad and forming the receiver below the second conductive signal pad.

38. The method of claim 29, further comprising:

masking respective surfaces of the first semiconductor device and the second semiconductor device;

forming recesses in the respective surfaces; and

depositing a conductive material into the recesses.

40. The method of claim 38, wherein masking respective surfaces further comprises applying a photoresist material to the respective surfaces, exposing the photoresist to radiation of a selected wavelength, and developing the photoresist.

41. A method of coupling a signal from a first semiconductor device to a second semiconductor device, comprising:

forming a layer of dielectric material having opposed first and second surfaces;

forming a first conductive signal pad on a surface of the first semiconductor device, the first conductive signal pad being in contact with the dielectric material adjacent the first surface of the layer of dielectric material;

forming a second conductive signal pad on a surface of the second semiconductor device, the second conductive signal pad being in contact with the dielectric material adjacent the second surface of the layer of dielectric material; the second conductive

signal pad being positioned in sufficient proximity to the first conductive signal pad to be capacitively coupled to the first conductive signal pad;

applying a first signal to the first conductive signal pad; and

coupling the first signal from the second conductive signal pad after the first signal has been capacitively coupled from the first signal pad to the second signal pad.

42. The method of claim 41, further comprising:

forming a transmitter in the first semiconductor substrate that is coupled to the first conductive signal pad; and

forming a receiver in the second semiconductor substrate that is coupled to the second conductive signal pad.

43. The method of claim 42, wherein forming a transmitter in the first semiconductor substrate comprises forming the transmitter at a position laterally adjacent to the first conductive signal pad; and forming a receiver in the second semiconductor substrate comprises forming the receiver at a position laterally adjacent to the second conductive signal pad.

44. The method of claim 42, wherein forming a transmitter in the first semiconductor substrate comprises forming the transmitter at a location below the first conductive signal pad; and forming a receiver in the second semiconductor substrate comprises forming the receiver at a location below the second conductive signal pad.

45. The method of claim 41, wherein forming a layer of dielectric material having opposed first and second surfaces comprises forming a layer of silicon dioxide.

46. The method of claim 41, wherein forming a layer of dielectric material having opposed first and second surfaces comprises forming a layer of silicon nitride.

47. The method of claim 41, further comprising forming a guard ring adjacent to at least one of the first conductive signal pad and the second conductive signal pad that is coupled to a ground potential.

48. The method of claim 47, wherein forming a guard ring adjacent to at least one of the first conductive signal pad and the second conductive signal pad further comprises forming a guard ring that substantially circumferentially surrounds at least one of the first conductive signal pad and the second conductive signal pad.

49. The method of claim 41, further comprising forming a ground plane adjacent to at least one of the first conductive signal pad and the second conductive signal pad that is coupled to a ground potential.

50. A method of coupling a signal from a first semiconductor device to a second semiconductor device, comprising:

placing a layer of dielectric material between respective surfaces of the first and second semiconductor devices; and

capacitively coupling a signal through the layer of dielectric material from the surface of the first semiconductor device to the surface of the second semiconductor device.

51. The method of claim 50, further comprising positioning a transmitter in the first semiconductor substrate; and forming a receiver in the second semiconductor substrate.

52. The method of claim 50, wherein placing a layer of dielectric material comprises forming a layer of silicon dioxide.

53. The method of claim 50, wherein placing a layer of dielectric material comprises forming a layer of silicon nitride.

54. A system in package device substantially as described herein with reference to Fig 2, 3 or 4 of the accompanying drawings.

55. A method of forming a system in package device, the method being substantially as described herein with reference to Fig 2, 3 or 4 of the accompanying drawings.

56. A method of coupling a signal from a first semiconductor device to a second semiconductor device, the method being substantially as described herein with reference to Fig 2, 3 or 4 of the accompanying drawings.

STRUCTURE AND METHOD FOR FORMING A CAPACITIVELY COUPLED CHIP-TO-CHIP SIGNALING INTERFACE

ABSTRACT OF THE DISCLOSURE

A system and method for providing capacitively-coupled signaling in a system-in-package (SiP) device is disclosed. In one embodiment, the system includes a first semiconductor device and an opposing second semiconductor device spaced apart from the first device, a dielectric layer interposed between the first device and the second device, a first conductive pad positioned in the first device, and a second conductive pad positioned in the second device that capacitively communicate signals from the second device to the first device. In another embodiment, a method of forming a SiP device includes forming a first pad on a surface of a first semiconductor device, forming a second pad on a surface of a second semiconductor device, and interposing a dielectric layer between the first semiconductor device and the second semiconductor device that separates the first conductive signal pad and the second conductive signal pad.

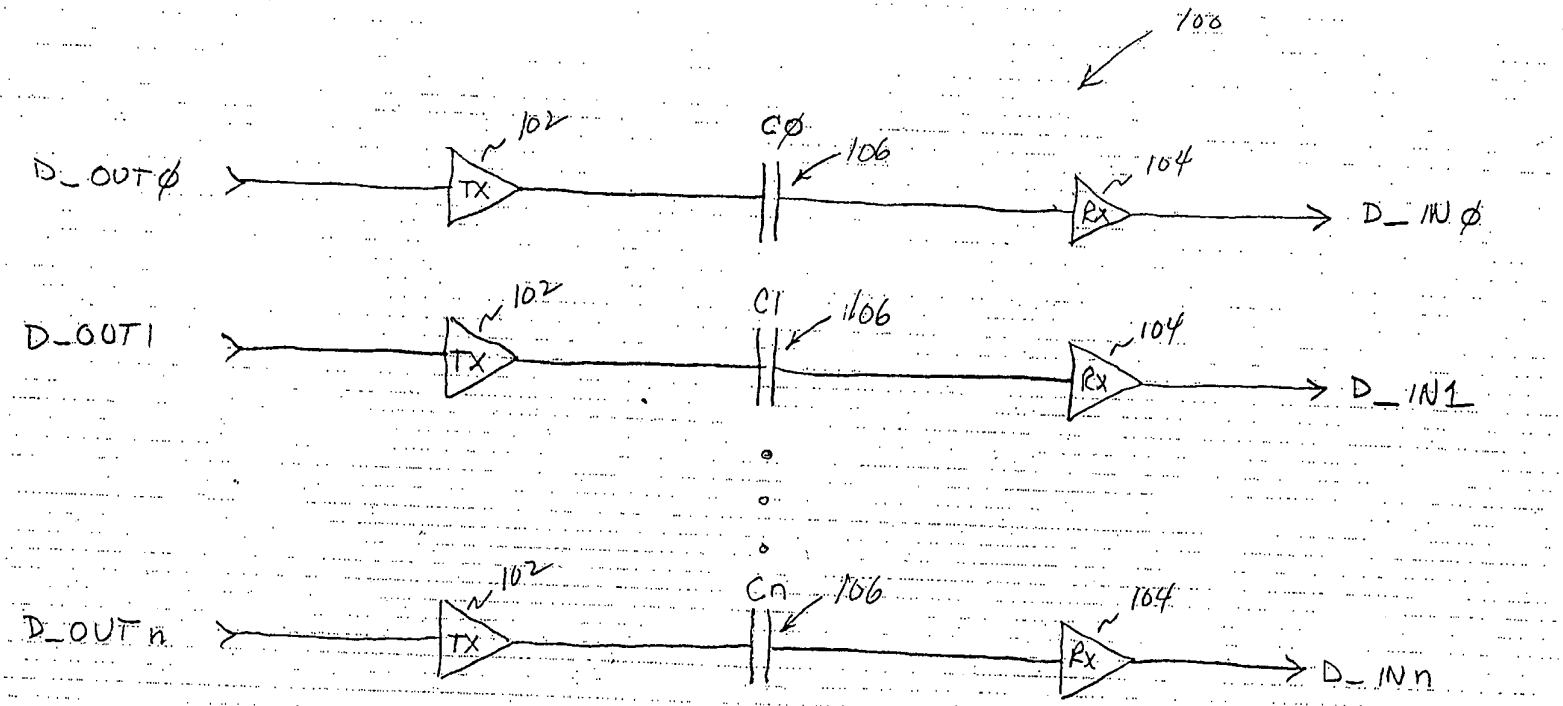


FIGURE 1

(PRIOR ART)

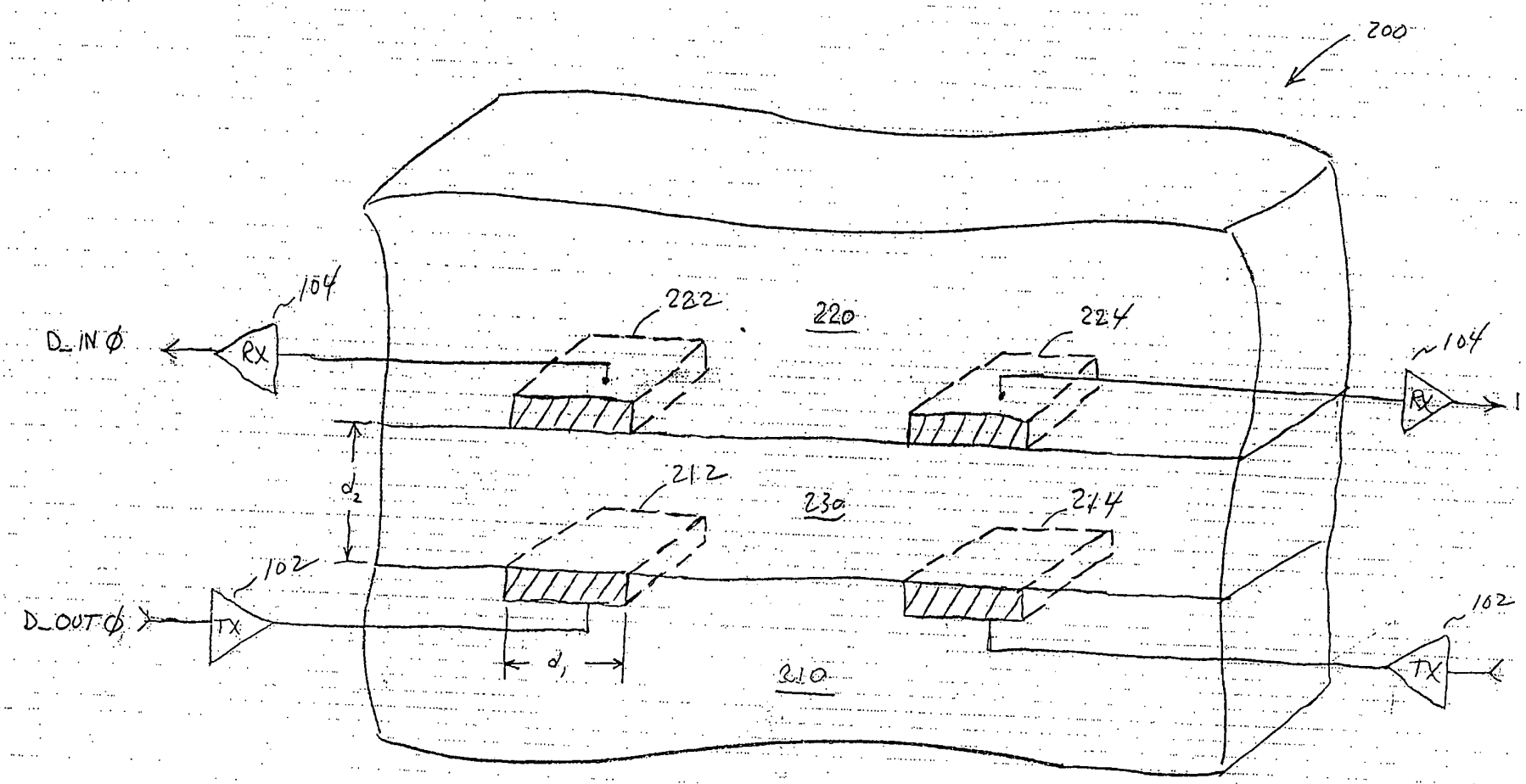
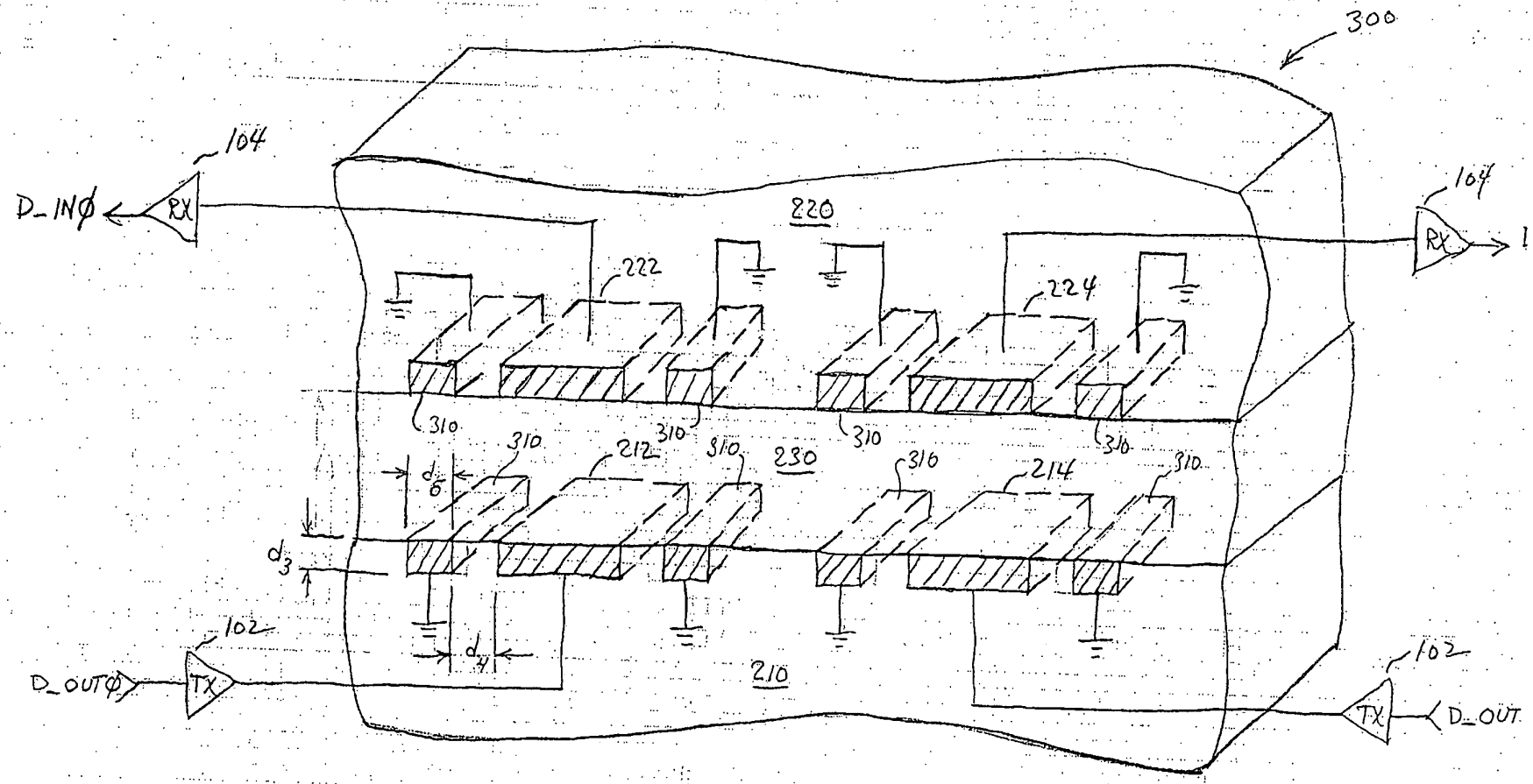

200
104
D_IN ϕ
RX
222
220
224
104
RX
212
230
214
102
D_OUT ϕ
TX
102
TX
210

FIGURE 2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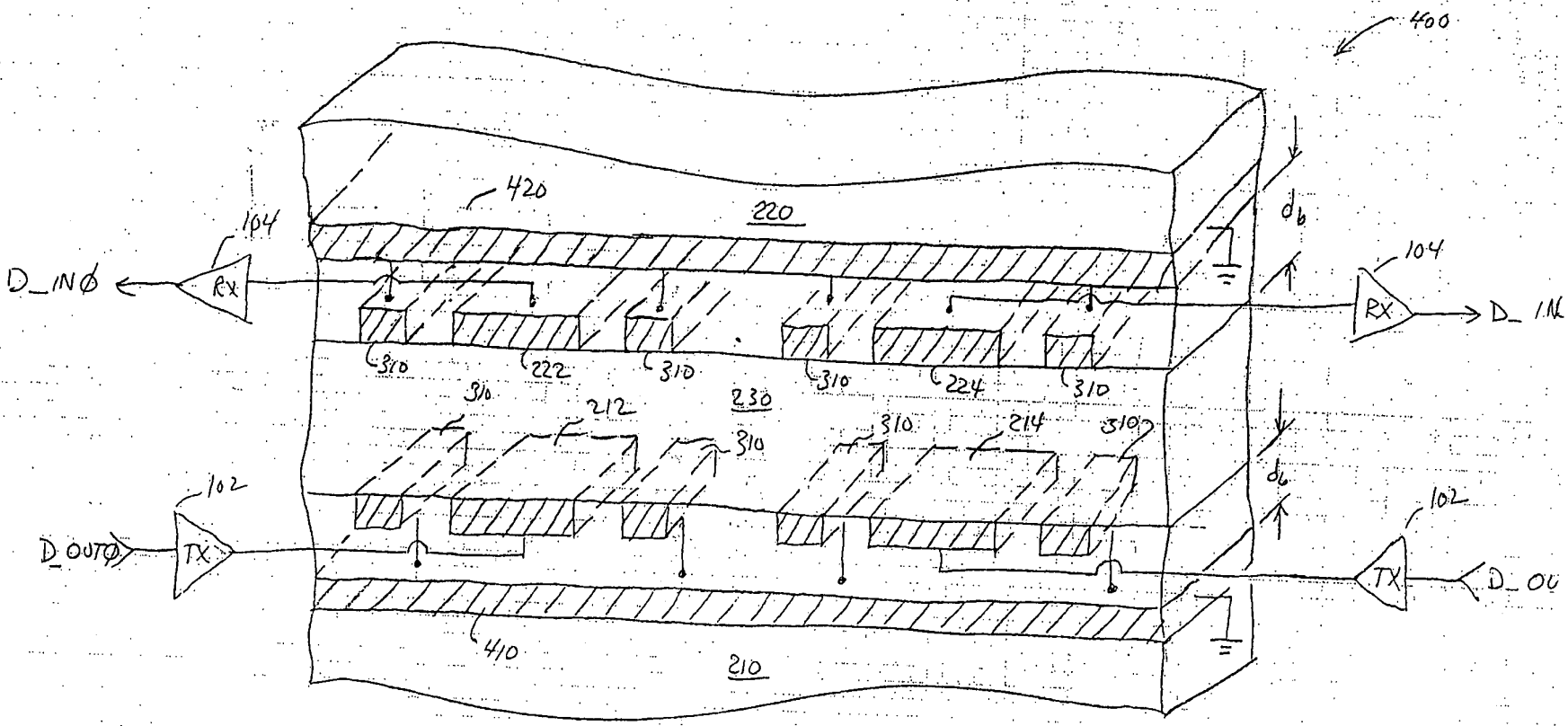
D_IN
RX
220
222
224
104
RX
1
310
310
310
310
310
310
212
214
230
d_6
d_3
d_4
102
D_OUT
TX
210
102
TX
D_OUT

FIGURE 3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420
220
104
RX
D_IN0
D_IN1
310
222
224
230
212
214
102
TX
D_OUT0
D_OUT1
410
210
d_6

FIGURE 4